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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/043,458	01/09/2002	Chin-Chi Teng	SILI 2282	6473

7812 7590 10/09/2003

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EXAMINER
WHITMORE, STACY

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 10/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/043,458	TENG ET AL.	
	Examiner	Art Unit	
	Stacy A Whitmore	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *16-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-5, and 9-13 rejected under 35 U.S.C. 103(a) as being unpatentable over Graef (US Patent 6,305,001) in view of Hathaway (US Patent 6,536,024).

2. As for claims 1 and 9, Graef taught the invention substantially as claimed, including

A method and computer-readable media containing a program which, when read and executed by a computer, causes the computer to synthesize a clock tree for a partitioned integrated circuit (IC) comprising a plurality of base level partitions and a top level partition each occupying a separate area of a semiconductor substrate, wherein the base level partitions comprise syncs to be clocked by edges of a clock signal applied to an entry node within the area occupied by the top level partition [abstract; col. 9, lines 11-32; col. 10, lines 11-28; col. 11, lines 6-9; col. 12, lines 6-56; fig.'s 6-7, and 9-10], the computer-readable media comprising:

first computer instructions for causing the computer to separately synthesize a plurality of independently balanced subtrees, each subtree corresponding to a separate base level partition and comprising a start point at a perimeter of the area occupied by that base level partition and a network of buffers and signal paths for conveying a clock signal edge from the start point to each sync included within that area [abstract; col. 9, lines 11-32; col. 10, lines 11-28; col. 11, lines 6-9; col. 12, lines 6-56; fig.'s 6-7, and 9-10]; and

second computer instructions for causing the computer to synthesize a top-level portion of the clock tree for conveying the clock signal from the entry point to the start point of each synthesized subtree [abstract; col. 9, lines 11-32; col. 10, lines 11-28; col. 11, lines 6-9; col. 12, lines 6-56; fig.'s 6-7, and 9-10].

Graef did not specifically disclose partitioning subtrees at the layout level.

Hathaway disclosed partitioning subtrees at the layout level [col. 30, line 45 – col.. 31, line 33].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Graef and Hathaway because partitioning at the layout level in Graef's system would have improved Graef's system by optimizing power consumption and clock skew which would improve cycle time to perform operation in the microprocessor design [see Hathaway, col. 31].

3. As for claims 2 and 10, Graef further taught

wherein each subtree has an average clock signal path delay that is an average of clock signal path delays between the subtree's start point and all syncs within the corresponding base level partition [fig. 7; col. 10; and fig. 9, clock distribution networks each have average clock delay of $\phi_{1,2,3}$; col. 13, line 46 – col. 14, line 37],

wherein at least two of the subtrees have substantially dissimilar average clock signal path delays [fig. 7; col. 10; and fig. 9, clock distribution networks each have average

clock delay of $\phi_{1,2,3}$ which is different in each network; and col. 13, line 46 – col. 14, line 37], and

wherein path delays of paths within the top level portion of the clock tree linking the entry node to the start point of each subtree compensate for differences in average path delays of the subtrees so as to substantially equalize clock signal path delays between the entry point and all syncs [fig. 7; col. 10; and fig. 9, clock distribution networks each have average clock delay of $\phi_{1,2,3}$; col. 13, line 46 – col. 14, line 37],

wherein at least two of the subtrees have substantially dissimilar average clock signal path delays [fig. 7; col. 10; and fig. 9, clock distribution networks each have average clock delay of $\phi_{1,2,3}$ which is different in each network; and col. 13, line 46 – col. 14, line 37].

4. As for claims 3 and 11, Graef further taught

wherein instructions for causing the computer to synthesize a balanced subtree of the clock tree for the top level partition for delivering the clock signal from a start point within the area of the substrate occupied by the top level partition to each sync included within the top level partition [col. 13, line 46 – col. 15, line 40; fig. 9];

wherein the synthesized top level portion of the clock tree also conveys the clock signal from the entry point to the start point of the synthesized subtree for the top level partition [col. 13, line 46 – col. 15, line 40; fig. 9].

5. As for claims 4 and 12, Graef further taught wherein the subtrees have substantially differing average clock signal path delays, each subtree's average clock signal path delay being defined as an average of clock signal path delays between that subtree's starting point and all syncs within the corresponding base level partition, and wherein the second computer instructions comprises:

computer instructions for causing the computer to select a first base level partition and a second base level partition from among the plurality of base level partitions,

computer instructions for causing the computer to synthesize a first signal path linking the start point of the subtree of first base level partition to a first node within the level partition, and

computer instructions for causing the computer to synthesize a second signal path linking the start point of the subtree of the second base level partition to the first node,

wherein the first and second signal paths provide substantially differing path delays between the first node and the start points of the subtrees of the first and second partitions to compensate for the substantially differing average clock signal path delay of the subtrees of the first and second base level partitions so that a clock signal edge departing the first node will arrive at each sync within the first and second base level partitions at substantially the same time [col. 13, line 46 – col. 15, line 40; fig. 9; especially col. 13, lines 50-54].

6. As for claims 5 and 13, Graef further taught wherein the second instructions cause the, computer to adjust path delays of the first and second signal paths to compensate for the substantially differing clock signal path delays of the subtrees of the first and second partitions by adjusting at least one of the following: a number of buffers included in the paths, a size of at least one buffer included in the path, a position of at least one buffer included in the path, and a position of the selected node relative to the start points of the first and second trees [col. 3, lines 39-67; col. 15, lines 1-42].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the

subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 6-8, and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Graef (US Patent 6,305,001) in view of Hathaway (USPatent 6,536,024) and further in view of Minami, " Clock tree synthesis based on RC delay balancing".

8. As for claims 6 and 14, Graef in view of Hathaway disclosed adjusting path delays by the number of buffers included in the paths [see as cited in the rejection of claims 5 and 13 above].

Graef in view of Hathaway did not specifically disclose all of the following: a number of buffers included in the paths, a size of at least one buffer included in the path, a position of at least one buffer included in the path, and a position of the selected node relative to the start points of the first and second trees.

Minami disclosed adjusting a position of at least one buffer included in the path, and a position of the selected node relative to the start points of the first and second trees.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Graef in view of Hathaway and Minami because both Graef in view of Hathaway and Minami disclose the adjusting of clock skew in paths and the addition of Minami's adjusting position and of a buffer and position of a node would have improved Graf's in view of Hathaway's system by adding more alternatives for adjusting clock signal path delays of subtrees thereby giving more ways to reduce clock skew.

Graef in view of Hathaway and Minami did not disclose adjusting the size of at least one buffer included in the path.

"Official Notice" is taken that both the concepts and advantages of adjusting the size of a buffer in a path are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include an adjustment of a buffer size in the system of Graef in view of Hatahway and Minami because adjusting the buffer size would have improved Graef in view of Minami's system by compensating for drive strength in circuit paths with large numbers of components.

9. As for claims 7 and 8, Graef in view of Hathaway and Minami disclosed the invention substantially as claimed, including computer instructions for causing the computer to select a third base level partition from among the plurality of base level partitions, computer instructions for causing the computer to synthesize a third signal path linking the first node to a second node within the top level partition, and computer instructions for causing the computer to synthesize a fourth signal path linking the subtree of --he third base level partition to the second node, wherein the third and fourth signal paths provide substantially differing path delays to compensate for substantially differing average clock signal path delays of the subtrees of the first, second and third partitions so that a clock signal edge departing the second node will arrive at each sync within the first, second and third partitions at substantially the same time [col. 13, line 46 – col. 15, line 40; fig. 9; especially col. 13, lines 50-54].

10. As for claim 8, Graef further disclosed wherein the second instructions cause the, computer to adjust path delays of the first and second signal paths to compensate for the substantially differing clock signal path delays of the subtrees of the first and second partitions by adjusting at least one of the following: a number of buffers included in the paths, a size of at least one buffer included in the path, a position of at least one buffer

included in the path, and a position of the selected node relative to the start points of the first and second trees [col. 3, lines 39-67; col. 15, lines 1-42].

11. Applicant's arguments with respect to claims 1-15 have been considered but are moot in view of the new ground(s) of rejection.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A Whitmore whose telephone number is (703) 305-0565. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Stacy A Whitmore
Patent Examiner
Art Unit 2812

SAW
September 30, 2003